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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,176	03/05/2002	Charles Patton	5181-84600	9947

7590 11/15/2005

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EXAMINER	
HARRISON, CHANTE E	

ART UNIT	PAPER NUMBER
2677	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,176	PATTON, CHARLES	
	Examiner	Art Unit	
	Chante Harrison	2677	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to communications: Request for Reconsideration, filed on 8/26/05. ***This action is made FINAL.***

2. Claims 18-40 are pending in the case. Claims 18, 26 and 34 are independent claims.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 18-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Debra Kipping et al., US 6,831,660 B1, 12/2004, and further in view of C. Narayanaswami, US 5,883,634, 3/1999.

As per independent claim 18, Kipping discloses passing the pixel location through a plurality of clip circuits (i.e. each clip register compares the pixel location to clip region boundaries to determine if the pixel is in inside, outside or on the region) (col. 4, ll. 60-65; col. 5, ll. 10-26), wherein the clip circuits are connected in a series to form a pipeline (Fig. 3 "310"), and wherein each clip circuit is a segment of the pipeline (Fig. 3 "310");

computing a window result in each clip circuit for the pixel location (col. 5, ll. 19-20), wherein each clip circuit is provided data defining a different one of the plurality of windows (Fig. 5 "504, 506, 508, 510"; col. 6, ll. 26-31), wherein the window result comprises an indication of inclusion of the pixel location within the corresponding one of the plurality of windows (col. 6, ll. 38-44).

Kipping fails to disclose outputting the pixel location and a window word from each clip circuit, wherein said outputting comprises, passing the pixel location and the window word directly to a next clip circuit in the series of clip circuits except for the last clip circuit in the series, and wherein the window word also comprises any previous window results; and examining the window word output by the last clip circuit in the series of clip circuits to determine if the pixel is included in at least one of the windows.

Narayanaswami discloses outputting the pixel location and a window word from each clip circuit (i.e. updates the clip buffer with the position and visibility data to be stored) (col. 1, ll. 30-40; col. 3, ll. 35-46), wherein said outputting comprises, passing the pixel location and the window word directly to a next clip circuit in the series of clip circuits except for the last clip circuit in the series (i.e. the clip buffer stores the visibility at each pixel position for each window; and updates the stored data upon any changes by any window) (col. 1, ll. 34-38; col. 3, ll. 38-40, 45-47), and wherein the window word also comprises any previous window results (i.e. the window manager maintains a clip mask of all visible regions from each window) (col. 3, ll. 42-45); and examining the window word output by the last clip circuit in the series of clip circuits to determine if the

pixel is included in at least one of the windows (i.e. before the drawing the pixel, testing the pixel position for a true, e.g. visible, value) (col. 3, ll. 49-53).

It would have been obvious to one of ordinary skill in the art to have the hardware clippers in graphics hardware of Kipping include outputting the pixel location and a window word from each clip circuit, wherein said outputting comprises, passing the pixel location and the window word directly to a next clip circuit in the series of clip circuits except for the last clip circuit in the series, and wherein the window word also comprises any previous window results; and examining the window word output by the last clip circuit in the series of clip circuits to determine if the pixel is included in at least one of the windows, as taught by Narayanaswami because window clipping management that updates a clip buffer with the position and visibility data to be stored for each window of a plurality of windows corresponds to outputting a pixel location and word defining pixel visibility for each window; and using the data as a mask of the visible data for any updated window visibility tests allows the pixel coordinates and pixel visibility to be passed along the pipeline of window clipping circuitry.

As per dependent claims 19 and 27, Kipping discloses said pixel location comprises a horizontal and a vertical coordinate that define position of said pixel on a screen (col. 4, ll. 60-66).

As per dependent claims 20, 28 and 35, Kipping discloses each of the plurality of windows comprises a first horizontal and a second horizontal coordinate and a first vertical and a second vertical coordinate that define each window's boundaries on the screen (col. 4, ll. 60-66; col. 7, ll. 35-40).

As per dependent claims 21 and 29, Kipping discloses wherein said computing window result computing horizontal inclusion by computing if said horizontal pixel coordinate is located between the first horizontal and the second horizontal coordinate of the corresponding window (i.e. determining to process graphics data within the clip region defined by min and max x coordinates) (col. 7, ll. 33-40); and computing vertical inclusion if said vertical pixel coordinate is located between the first vertical and the second vertical coordinate of the corresponding window (i.e. determining to process graphics data within the clip region defined by min and max y coordinates) (col. 7, ll. 3-40).

As per dependent claims 22 and 30, Kipping discloses wherein said computing window result further comprises: setting the indication of inclusion of the pixel to positive if both the horizontal and vertical inclusions are true (i.e. draw region) (col. 4,ll. 60-66; col. 5, ll. 20-25), and setting the indication of inclusion to negative if one or more of the horizontal and vertical inclusions are false (i.e. no draw) (col. 4, ll. 60-66; col. 5, ll. 24-27).

As per dependent claims 23, 31 and 36, Kipping discloses setting a no draw setting for a pixel outside of a window region (col. 5, ll. 17-22); and drawing pixels determined to be within or on the window region (col. 5, ll. 17-24).

Kipping fails to disclose clipping the pixel if said examining determines that the pixel is not included in any of the plurality of windows, and propagating the pixel if said examining determines that the pixel is included in at least one of the plurality of windows, which Narayanaswami respectively discloses (col. 2, ll. 23-27; col. 3, ll. 48-56).

Narayanaswami teaches a window manager for maintaining a clip mask of all visible regions for each window, such that a window's visible regions are stored and updated using a clip buffer; and only pixel's that are visible are drawn.

It would have been obvious to one of skill in the art to have the hardware clipping circuit of Kipping include clipping a pixel not included in any of the windows and propagating a pixel included in at least one of the windows as taught by Narayanaswami because determining, storing and updating visible pixels included in the plurality of windows enables clipping a pixel not included in a window, as the pixel is not visible in the window, and drawing any pixel that is included in the window, as the pixel is visible.

As per dependent claims 24, 32 and 37, Kipping discloses wherein said plurality of windows comprise two or more 2-D windows (col. 6, ll. 1-5).

As per dependent claims 25, 33 and 38,Kipping discloses wherein said plurality of clip circuits are identical circuits (Fig. 3 "310").

As per independent claim 26, Kipping discloses supplying window boundary coordinates for a different one of a plurality of windows to each clip circuit of a plurality of clip circuits connected in a series (col. 6, ll. 1-5; col. 7, ll. 33-38); determining inclusion of a pixel in the corresponding window in each clip circuit (col. 4, ll. 60-65).

Kipping fails to disclose passing the pixel and a result of said determining inclusion to a next clip circuit in the series of clip circuits, except for a last clip circuit of the series of clip circuits.

The rationale as applied in the rejection of independent claim 18 applies herein.

As per independent claim 34, Kipping discloses a plurality of clip circuits connected in a series (Fig. 3 "310"), wherein each circuit in the series is configured to: (a) receive horizontal and vertical coordinates locating a pixel (col. 4, ll. 57-63), (b) receive horizontal and vertical coordinates defining a different one of a plurality of windows (col. 6, ll. 50-52; col. 7, ll. 33-38), (c) compute a window result indicating inclusion of the pixel within the corresponding window defined in (b) (col. 4, ll. 60-65).

Kipping fails to disclose except for a last clip circuit in the series, (d) pass the horizontal and vertical coordinates of the pixel, the window result computed in (c), and any prior window results to a next clip circuit in the series of clip circuits.

The rationale as applied in the rejection of independent claim 18 applies herein.

As per dependent claim 39, Kipping discloses wherein each clip circuit of the plurality of clip circuits is directly connected to the next clip circuit in the series of clip circuits (Fig. 3 "310").

As per dependent claim 40, Kipping discloses wherein the plurality of clip circuits form a pipeline, and each clip circuit is a segment of the pipeline (Fig. 3 "310").

Response to Arguments

1. Applicant's arguments filed 8/26/05 have been fully considered but they are not persuasive.

Regarding claim 18, Applicant argues (pp. 8, Para 1) Kipping does not teach the clip circuits are connected in a series to form a pipeline, and wherein each clip circuit is a segment of the pipeline.

In reply, Kipping teaches performing computations in a graphic system having a graphic adapter that includes a pipeline for partitioning processing elements, which include clipping functions performed by hardware clippers, into stages that execute sequentially (col. 1, ll. 45-68). Therefore Kipping teaches clip circuits as he teaches a plurality of hardware clippers. Kipping teaches the clip circuits are connected in series as he teaches hardware clippers connected in a pipeline and executing sequentially. Kipping also teaches each clip is a segment of the pipeline as he teaches the graphics pipeline is used to partition processing elements, which include clipping functions performed in hardware, into stages, such that each hardware clipper is a segment of the pipeline.

Regarding claim 18, Applicant argues (pp. 8, Pare 2) Kipping and Narayanaswami do not teach outputting the pixel location and a window word from each clip circuit, wherein

outputting comprises, passing the pixel location and the window word directly to a next clip circuit.

In reply, Kipping teaches the graphics adapter including a clipping buffer (Fig. 3) and using the clipping buffer, i.e. a hardware clipping plane, to determine the graphic data to display (col. 4, ll. 52-67). Narayanswami teaches the clip buffer stores the visibility at each pixel position for each window, and updates the stored data upon any changes by any window as each window makes a comparison to the clip buffer value (col. 1, 11. 34-38, col. 3, 11. 38-40, 45-47). Thus, in teaching the clip buffer stores the pixel visibility value for each window, where each window makes a comparison of the visibility of its region to the value of the clip buffer, such that the clip buffer values are updated by each window comparison, Narayanaswami teaches outputting the pixel location and visibility value for each clip buffer and passing the pixel location and value to a next clip circuit. It would have been obvious to include the teachings of Narayanaswami with the method of Kipping because the clip buffer corresponds to a hardware clipping plane, where each clipping plane indicates the pixel visibility within its display region, which enables control over which hardware clipper will write or overwrite the data to be displayed.

Regarding claim 18, Applicant argues (pp. 8, Para 5) Kipping and Narayanaswami do not teach examining the window word output by the last clip circuit in the series to determine if the pixel is included in at least one of the windows.

In reply, Kipping teaches performing computations in a graphic system having a graphic adapter that includes a pipeline for partitioning processing elements, which include clipping functions performed by hardware clippers, into stages that execute sequentially (col. 1, ll. 45-68). Kipping teaches the graphics adapter including a clipping buffer (Fig. 3) and using the clipping buffer, i.e. a hardware clipping plane, to determine by a comparison of regions the graphic data to display (col. 4, ll. 52-67), such that the clipping planes having pixels that fall within the region write data to the frame buffer for display. Narayanaswami teaches window clipping is performed by hardware in a graphics pipeline in a graphics adapter (col. 1, ll. 35-40). Narayanaswami teaches maintaining the clipping window for each window in memory for update and access of pixel visibility such that before drawing a pixel for a window, the pixel position is tested for a true, e.g. visible, value (col. 3, 11. 49-53). It would have been obvious to include the examination of the window word as taught by Narayanaswami with the method of Kipping because both make comparisons of currently processing and previously stored clipping buffer/plane values to determine which pixels are included within the window region and should be written to the frame buffer for display, such that the last clipping buffer/plane comparison indicates that the included pixel output from the comparison originates from any one of the previously compared clipping buffer/planes.

Conclusion

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chante Harrison whose telephone number is 571-272-7659. The examiner can normally be reached on Monday, Tuesday and Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chante Harrison
Examiner
Art Unit 2677

Ch
November 1, 2005

AMR A. AWAD
PRIMARY EXAMINER